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Description

Field Effect-Controlled Semiconductor Component

This invention relates to a field effect-controlled semiconductor component according to the preamble of Claim 1.

Such a field effect-controlled semiconductor component is, for example, a vertical MOS field effect transistor. These transistors have been known for a long time and are described, for example, in the Siemens Datenbuch [Siemens Data Book] 1993-94 SIPMOS Semiconductors, Power Transistors and Diodes, pages 29 ff. Figure 4 on page 30 of this Siemens Data Book shows the basic design of such a power transistor. With such a transistor, the n^+ substrate is the carrier with the drain metallization beneath it. Above the n^+ substrate there is an n^--epitaxial layer that may have different thicknesses, depending on the blocking voltage, and is doped accordingly. The gate of n^+ polysilicon above that is embedded in insulating silicon dioxide and serves as an implantation mask for the p trough and for the n^- source region. The source metallization covers the entire structure and connects the individual transistor cells of the chip in parallel. Additional details can be found on pages 30 ff. of the Siemens Data Book.

One disadvantage of such an arrangement is that the on-state resistance R_{on} of the drain source load region increases with an increase in the dielectric strength of the semiconductor component because the thickness of the epitaxial layer must increase. At 50 V, the on-state resistance R_{on} per unit of area is approximately 0.20 Ωmm^2 and increases to a value of approximately 10 Ωmm^2 at a blocking voltage of 1000 V, for example.

To solve this problem, the IGBT was developed, combining MOS and epola functions to improve their conductivity. However, such a transistor is slower than a MOSFET.

It is known that, with lateral field effect transistors, the gate may be designed so that it increases linearly or in steps, for example, in the direction of the drain electrode, whereby the breakdown voltage increases with an increase in the distance of the gate electrode from the channel region and the saturation voltage also increases. Due to such a design, an iterative network of a plurality of field effect transistors with increasing breakdown voltages and lower saturation voltages is implemented in principle. However, lateral transistors require a large area.

U.S. Patent 5,216,275 describes a semiconductor component in which the drain layer applied to the substrate consists of vertical alternating p- and n-doped layers. U.S. Patent 5,216,275 shows these layers in Figure 4 of the description, for example. The p layers are labeled as 7 and the n layer as 6. It is stated in the description, in particular column 2, line 8, that the alternating p- and n-type layers must each be connected to the p^+ and p^- regions. However, this results in a great restriction in the design of a semiconductor component, because the edge areas can no longer be designed freely.

U.S. Patent 5,438,215 describes a high-blocking power MOSFET, which has a reduced on-state resistance. However, such a component is difficult to manufacture.

Therefore the object of the present invention is to provide a novel field effect-controlled semiconductor component which will provide a low on-state resistance despite having a high blocking voltage.

This object is achieved through the characterizing part of Claim 1. Embodiments and characteristics are described in the subclaims.

The advantage of the present invention is that the aforementioned advantages of a lateral field effect transistor can also be utilized according to this invention with a vertical field effect transistor by increasing the distance of the gate and/or insulated additional magnetoresistor electrode, which is introduced into the substrate in the vertical direction, from the surrounding insulating gate oxide with an increase in depth.

Another advantage is that such a trench structure can be arranged in the form of a grid or strips around the individual transistor cells, thus permitting an optimum influence on the space charge region.

Depending on the design of the vertical additional electrode, it may be connected electrically to the source or gate or it may also be designed so that it either forms a part of the gate electrode or is the gate electrode itself.

This invention is explained in greater detail below on the basis of five figures, in which

Figure 1 shows a first exemplary embodiment of an inventive vertical MOS field effect transistor,
Figure 2 shows a detail of a top view of an inventive field effect transistor according to Figure 1,
Figure 3 shows a second exemplary embodiment of an inventive MOS field effect transistor,
Figure 4 shows a third exemplary embodiment of an inventive MOS field effect transistor and
Figure 5 shows a detail of a trench structure of another inventive MOS field effect transistor.

The vertical MOSFET shown in Figure 1 has an n^+-doped substrate which is provided with a drain terminal, e.g., metallization, on the rear side. An n^--doped epitaxial layer 2 into which

p-doped source regions 3 are introduced is deposited above this layer 1. These p-doped source regions 3 have embedded n^+ regions 4. A source metallization 7 forms a short circuit between this n^+ - and the p-doped source region 3, 4. Figure 1 shows two of these source regions 3, 4, which are arranged with a distance between them and whose intermediate region in combination with the drain regions 1, 2 defines a channel above which a gate 6 embedded in gate oxide 5 is situated.

Beneath the gate, a trench-like recess extends in the epitaxial layer 2 with an auxiliary electrode 10b surrounded by insulating gate oxide 9b within the trench. This auxiliary electrode 10b is designed in the form of a wedge so that the thickness of the insulating gate oxide 9b increases with an increase in distance from the surface facing the gate into the epitaxial layer 2. In the example shown here, the distance d1 is thus smaller than the distance d2 and the distance d3. In the exemplary embodiment depicted according to Figure 1, the trench walls 11b also have n^+ doping. In addition to the trench structure 8b beneath the gate, a similar trench structure is also provided beneath the source electrode. The trench 8a formed there extends from the source metallization 13 through the source region 3 in the direction of the drain through the epitaxial layer 2. The additional electrode designed in the form of a wedge extends here from the source metallization to which it is electrically connected in the direction of the drain in the same way as the auxiliary electrode 10b. The trench walls 11a again have n^+ doping beginning beneath the source electrode 3.

Figure 2 shows how the auxiliary electrodes 10a and 10b can be connected to one another and to the source regions. The auxiliary electrodes 10a and 10b and additional auxiliary electrodes not shown in Figure 1 form a grid-like structure which first surrounds the source regions and additionally crosses the source regions. Then as depicted in Figure 1, the additional auxiliary

electrodes 10a, 10b are connected to the source metallization through individual source cells. Of course all the auxiliary electrodes that cross through the source regions are each connected to the source metallization. At the points of intersection of the auxiliary electrodes 10a and 10b which are designed in the form of a grid, the auxiliary electrodes are also joined together and thus form a ring-shaped structure surrounding the individual transistor cells. A strip structure is also possible.

The mechanism of action of such a vertical MOSFET corresponds essentially to that of the known lateral MOSFETs with an additional magnetoresistor, whose distance from the epitaxial layer increases in the direction of the drain.

Figure 3 shows another exemplary embodiment where the auxiliary electrode is also designed in a wedge shape in the vertical direction but is connected directly to the gate 6. The same elements have the same reference numbers here. The additional wedge-shaped auxiliary electrode 13 here is thus part of the gate and is thus completely embedded in the gate oxide 5 as well as the gate oxide 12 of the trench 8. The trench extends here into the substrate 1, whereby only the side walls 14 have n^+ doping in this exemplary embodiment.

Figure 4 shows another embodiment of the arrangement depicted in Figure 3, whereby the trench technology known from memory technology is used. The difference in comparison with trenches known in the past is that the combined gate-magnetoresistors are here again partially designed with a wedge shape, so that the gate oxide 12 surrounding them increases in thickness in the direction of the drain. This combined gate-magnetoresistor structure is labeled as 15 in Figure 4. The wedge-shaped design begins here approximately starting at the end of the source region 3 and extends in the direction of the drain terminal.

The n^+ layer implanted outside of the trench has a doping of less than approximately 10^{12} $1/cm^2$. It should be high enough so that, when completely emptied, there is no avalanche breakdown in the layers 14. As explained here, the additional auxiliary electrodes may be made of n^+ polysilicon and their connection may be to the source contact or to the gate terminal.

Figure 5 shows a detail of the trench structure according to Figure 3. In addition, another p-doped layer 16 is also introduced here into the edge area of the trench. A plurality of alternating p- or n-doped layers may also be introduced or the arrangement according to Figure 5 may be switched so that the n^+ layer 14 is on the inside and the p layer 16 is on the outside. The layer 16 may also be created by ion implantation.

The inventive structures have been explained as n-channel FET but they may equally be implemented with corresponding reverse doping in a p-channel version. The edge of transistors constructed in this way may be designed as it is with the power MOSFETs conventional at the present time.

The doping of the trench walls 11a, 11b, 14, 16 may be accomplished by ion implantation at an angle to the trench wall. It should be high enough that there is no avalanche breakdown in the layers 14 when completely emptied.

Patent Claims

1. Field effect-controlled semiconductor component comprising
- a drain region of the first conduction type,
- at least one gate electrode consisting of a polycrystalline silicon, whereby this is insulated with respect to the drain region,
- at least one source region of the second conduction type introduced into the drain region,

characterized in that

the drain region has at least one trench structure (8, 8a, 8b) introduced into it, extending from the surface of the semiconductor component into the drain region (2, 1) within which a magnetoresistor (10a, 10b, 13, 15) surrounded by an oxide layer (9a, 9b, 12) is introduced, whereby the thickness of the oxide layer (9a, 9b, 12) increases in the direction of the drain electrode.

2. Field effect-controlled semiconductor component according to Claim 1,

characterized in that

the oxide layer (9a, 9b, 12) surrounding the magnetoresistor is surrounded by a layer (11a, 11b, 14) more strongly doped by the first conduction type in comparison with the drain region (2).

3. Field effect-controlled semiconductor component according to Claim 2,

characterized in that

at least one additional layer (16) of the second conduction type is introduced into the oxide layer (9a, 9b, 12) surrounding the magnetoresistor.

4. Field effect-controlled semiconductor component according to one of the preceding claims,

characterized in that

a plurality of trench structures (8a, 8b, 8) is arranged in a grid or strip pattern in the semiconductor component.

5. Field effect-controlled semiconductor component according to one of the preceding claims,
characterized in that
the magnetoresistor (10a, 10b) is electrically connected to the source terminal (s).

6. Field effect-controlled semiconductor component according to one of Claims 1 through 4,
characterized in that
the magnetoresistor (13, 15) is electrically connected to the gate electrode (G).

7. Field effect-controlled semiconductor component according to Claim 6,
characterized in that
the magnetoresistor (15) is designed to be vertical and it functions as a gate at the same time.

8. Field effect-controlled semiconductor component according to one of Claims 1 through 6, characterized in that the magnetoresistor is made of polysilicon.